MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

EEN7036 – DEVICE PROCESSING AND TECHNOLOGY

(M.Eng in Microelectronics)

12 MARCH 2016
2.30 p.m - 5.30 p.m
(3 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 7 pages with 4 Questions only.

2. Attempt **ALL** questions . All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

QUESTION 1

(a) After removal from the crystal grower, the silicon crystal goes through a series of steps that result in the finished wafer. Briefly describe each of these steps.

[11 marks]

(b) The design of clean room is important in producing contamination-free wafers. There are four distinct clean-room design strategies to be considered, namely, Clean Work Station, Tunnel Design, Total Clean Room, and Micro- and Mini-Environments. Discuss the concept of "Micro- and Mini-Environments" strategy adopted in the design and construction of the clean room.

[7 marks]

(c) Imagine, you are a consultant for a clean room design film, and you were approached by a representative from a semiconductor industry which is venturing into Power Metal Oxide Semiconductor Field-Effect Transistors (Power MOSFETs) technology. You are required to come out with design on the clean room suitable for the production activities for the Power MOSFETs. Describe and justify your clean room designs, which include the "class" of the clean room, and the main equipment to be located in the new clean room.

[7 marks]

Continued .....

QUESTION 2

(a) During diffusion process, at high temperatures (900°C to 1200°C), the dopant atoms move from the silicon surface into the silicon crystal via vacancy and interstitial diffusion mechanisms. With neat schematic sketches, discuss the vacancy and interstitial diffusion mechanisms and compare the characteristics of these two diffusion mechanisms.

[8 marks]

(b) A p-n junction is formed at 1000 °C by diffusing boron atoms into an n-type semiconductor having concentration of 1×10^{16} cm^{-3}. The surface concentration of boron in the semiconductor, C_S, is 1×10^{18} cm^{-3} and it is solubility limited. The diffusivity of boron in the semiconductor is 1.5×10^{-13} cm^2s^{-1} at 1000 °C and the diffusion time is 8 minutes. Determine the junction depth of the p-n junction. The Error Function Table (Table 1) is given in the appendix of this question paper.

[10 marks]

(c) With schematic aids, describe how an ion implantation technique can be used in the Separation by Implantation of Oxygen (SIMOX) process in the fabrication of silicon on insulator (SOI) wafers. [7 marks]

Continued .....

QUESTION 3

(a) Describe the properties of four basic ingredients in the photoresist solution for photolithographic patterning process.

[4 marks]

(b) Given a projection lithographic system with a resist constant, K, of 0.9 and a numerical aperture, NA, of 0.2. Determine the minimum structure size achievable with lithographic exposure wavelengths of 80, 150, 220, and 300 nm, respectively. Among these exposure wavelengths, suggest the suitable exposure wavelength(s) for the patterning of devices with structure size limited to below 1 μm.

[5+1 marks]

(c) Describe the physical mechanisms of a wet etching process.

[5 marks]

(d) Discuss the advantages and disadvantages of dry etching techniques.

[5+1 marks]

(e) Propose the type of dry etcher (reactive ion etcher or sputter etcher) you would adopt in the following scenarios. Provide justifications for your proposals.

(i) Anisotropic etching of a thick film on a thick insulating layer. [2 marks]

(ii) Etching of a 1000 Å chromium gate metal for a transistor having an underlying insulating layer of 40 Å with large channel length and channel width. [2 marks]

Continued .....

QUESTION 4

As a design engineer in semiconductor film, you are required to design a mask set and patterning steps for a complementary metal-oxide semiconductor (CMOS) gate as given in Figure Q4 below. The CMOS gate consists of an n-channel and a p-channel transistors fabricated on p-type substrate. The transistors constitutes of metal layers as polysilicon gate and drain/source contact electrodes, silicon oxide as field and gate oxide, and nitride as spacer layer.

(a) Design a patterning process for the CMOS gate. With neat sketch, describe your design processing flow.

[12 marks]

(b) How many masks are required in the patterning of the CMOS gate?

[3 marks]

(c) Explain the functionalities of the following constituents in the fabrication processing of the CMOS gate.

(i) Nitride spacer in the CMOS processing. [2 marks]

(ii) Polysilicon gate instead of metal gate. [2 marks]

(iii) Refractory metal layers on top of the gate, source and drain regions.

[3 marks]

(iv) Low source and drain implant concentration. [3 marks]

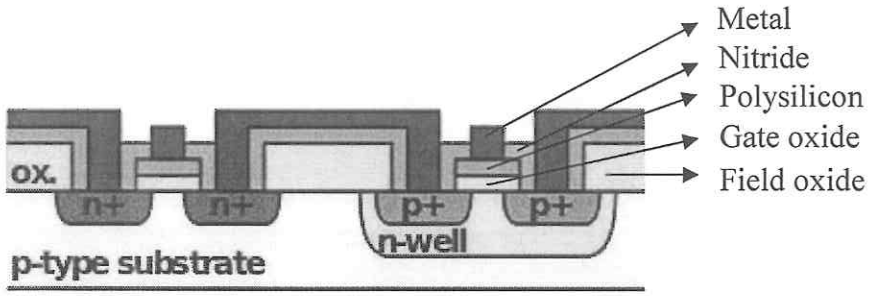

Figure Q4: Schematic cross-section of a CMOS gate.

End of Question

Appendix

Table 1

Values of the error function $\operatorname{erf}(t) = \frac{2}{\sqrt{\pi}} \int_0^t e^{-a^2} da$

t	0	1	2	3	4	5	6	7	8	9
0.0	0.000	0.0113	0.0226	0.0338	0.0451	0.0564	0.0676	0.0789	0.0901	0.1013
0.1	0.1125	0.1236	0.1348	0.1459	0.1569	0.1680	0.1790	0.1900	0.2009	0.2118
0.2	0.2227	0.2335	0.2443	0.2550	0.2657	0.2763	0.2869	0.2974	0.3079	0.3183
0.3	0.3286	0.3389	0.3491	0.3593	0.3694	0.3794	0.3893	0.3992	0.4090	0.4187
0.4	0.4284	0.4380	0.4475	0.4569	0.4662	0.4755	0.4847	0.4937	0.5027	0.5117
0.5	0.5205	0.5292	0.5379	0.5465	0.5549	0.5633	0.5716	0.5798	0.5879	0.5959
0.6	0.6039	0.6117	0.6194	0.6270	0.6346	0.6420	0.6494	0.6566	0.6638	0.6708
0.7	0.6778	0.6847	0.6914	0.6981	0.7047	0.7112	0.7175	0.7238	0.7300	0.7361
0.8	0.7421	0.7480	0.7538	0.7595	0.7651	0.7707	0.7761	0.7814	0.7867	0.7918
0.9	0.7969	0.8019	0.8068	0.8116	0.8163	0.8209	0.8254	0.8299	0.8342	0.8385
1.0	0.8472	0.8468	0.8508	0.8548	0.8586	0.8624	0.8661	0.8698	0.8733	0.8768
1.1	0.8802	0.8835	0.8868	0.8900	0.8931	0.8961	0.8991	0.9020	0.9048	0.9076
1.2	0.9103	0.9130	0.9155	0.9181	0.9205	0.9229	0.9252	0.9275	0.9297	0.9319
1.3	0.9340	0.9361	0.9381	0.9400	0.9419	0.9438	0.9456	0.9473	0.9490	0.9507
1.4	0.9523	0.9539	0.9554	0.9569	0.9583	0.9597	0.9611	0.9624	0.9637	0.9649
1.5	0.9661	0.9673	0.9684	0.9695	0.9706	0.9716	0.9726	0.9736	0.9746	0.9755
1.6	0.9764	0.9772	0.9780	0.9789	0.9796	0.9804	0.9811	0.9818	0.9825	0.9832
1.7	0.9838	0.9844	0.9850	0.9856	0.9861	0.9867	0.9872	0.9877	0.9882	0.9886
1.8	0.9891	0.9895	0.9899	0.9904	0.9907	0.9911	0.9915	0.9918	0.9922	0.9925
1.9	.99279	.99309	.99338	.99366	.99392	.99418	.99443	.99466	.99489	.99511
2.0	.99532	.99552	.99572	.99591	.99609	.99626	.99642	.99658	.99673	.99688
2.1	.99702	.99715	.99728	.99741	.99753	.99764	.99775	.99785	.99795	.99805
2.2	.99814	.99822	.99831	.99839	.99846	.99854	.99861	.99867	.99874	.99880
2.3	.99886	.99891	.99897	.99902	.99906	.99911	.99915	.99920	.99924	.99928
2.4	.99931	.99935	.99938	.99941	.99944	.99947	.99950	.99952	.99955	.99957
2.5	.99959	.99961	.99963	.99965	.99967	.99969	.99971	.99972	.99974	.99975
2.6	.99976	.99978	.99979	.99980	.99981	.99982	.99983	.99984	.99985	.99986
2.7	.99987	.99987	.99988	.99989	.99989	.99990	.99991	.99991	.99992	.99992
2.8	.99992	.99993	.99993	.99994	.99994	.99994	.99995	.99995	.99995	.99996
2.9	.99996	.99996	.99996	.99997	.99997	.99997	.99997	.99997	.99997	.99998
3.0	.99998	.99998	.99998	.99998	.99998	.99998	.99998	.99999	.99999	.99999

for $t > 3$ $\quad \operatorname{erf}(t) \approx 1 - \frac{1}{\sqrt{\pi}\, t} \exp\left(-t^2\right)$

$\operatorname{erfc}(t) = 1 - \operatorname{erf}(t)$

Continued .....

List of Equations

$$C(x,t) = C_s erfc\left[\frac{x}{2\sqrt{Dt}}\right]$$

$$N(x) = \frac{Q_o}{\sqrt{2\pi}\Delta R_p}\exp\left[-\frac{1}{2}\left(\frac{x-R_p}{\Delta R_p}\right)^2\right]$$

$$X_j = R_P \pm \Delta R_P\sqrt{2\ln(N_P/N_B)}$$

$$Q = \int_0^\infty C(x,t)dx = 2Cs\sqrt{\frac{Dt}{\pi}}$$

$$W_{min} \approx [K\lambda g]^{1/2}$$

$$C(x,t) = \frac{Q_T}{\sqrt{\pi Dt}}e^{-\frac{x^2}{4Dt}} t > 0$$

$$W_{min} \approx K\{\lambda/NA\}$$

$$C_s = \frac{Q}{\sqrt{\pi Dt}}$$

$$x_j = 2\sqrt{Dt\ \ln(N_0/N_B)}$$

$$x_j = 2\sqrt{Dt}\ erfc^{-1}(N_B/N_0)$$

$$Q = \frac{1}{qA}\int Idt$$

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